FIG. 1

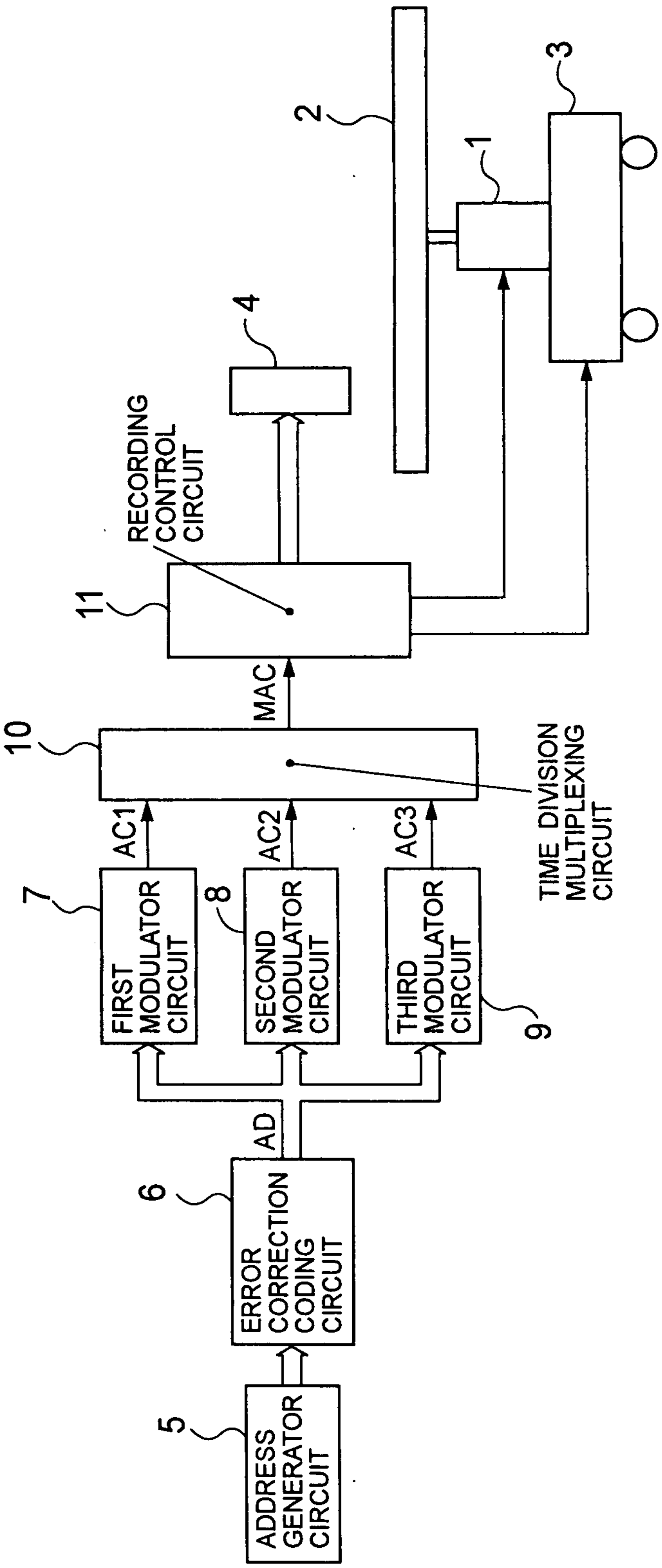

ADDRESS GENERATOR CIRCUIT
5
ERROR CORRECTION CODING CIRCUIT
6
AD
FIRST MODULATOR CIRCUIT
7
SECOND MODULATOR CIRCUIT
8
THIRD MODULATOR CIRCUIT
9
AC1
AC2
AC3
10
TIME DIVISION MULTIPLEXING CIRCUIT
MAC
11
RECORDING CONTROL CIRCUIT
4
2
1
3

FIG. 2

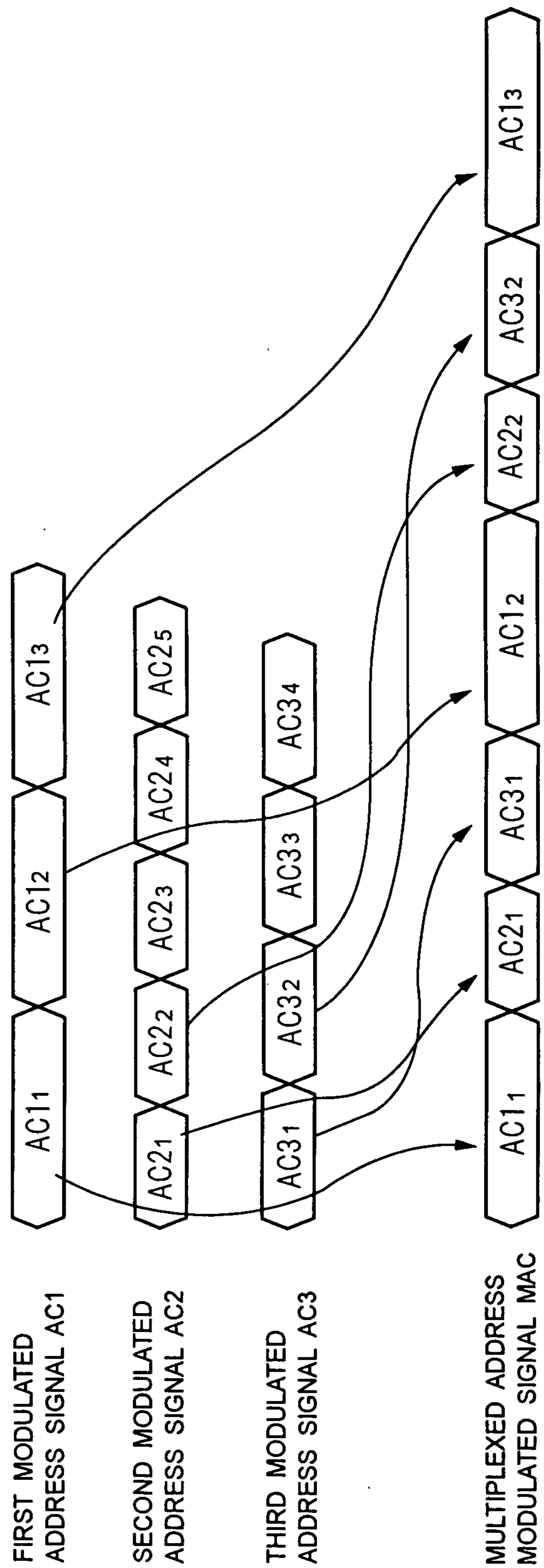

FIRST MODULATED ADDRESS SIGNAL AC1
SECOND MODULATED ADDRESS SIGNAL AC2
THIRD MODULATED ADDRESS SIGNAL AC3
MULTIPLEXED ADDRESS MODULATED SIGNAL MAC
$AC1_1$
$AC1_2$
$AC1_3$
$AC2_1$
$AC2_2$
$AC2_3$
$AC2_4$
$AC2_5$
$AC3_1$
$AC3_2$
$AC3_3$
$AC3_4$
$AC1_1$
$AC2_1$
$AC3_1$
$AC1_2$
$AC2_2$
$AC3_2$
$AC1_3$

FIG. 3

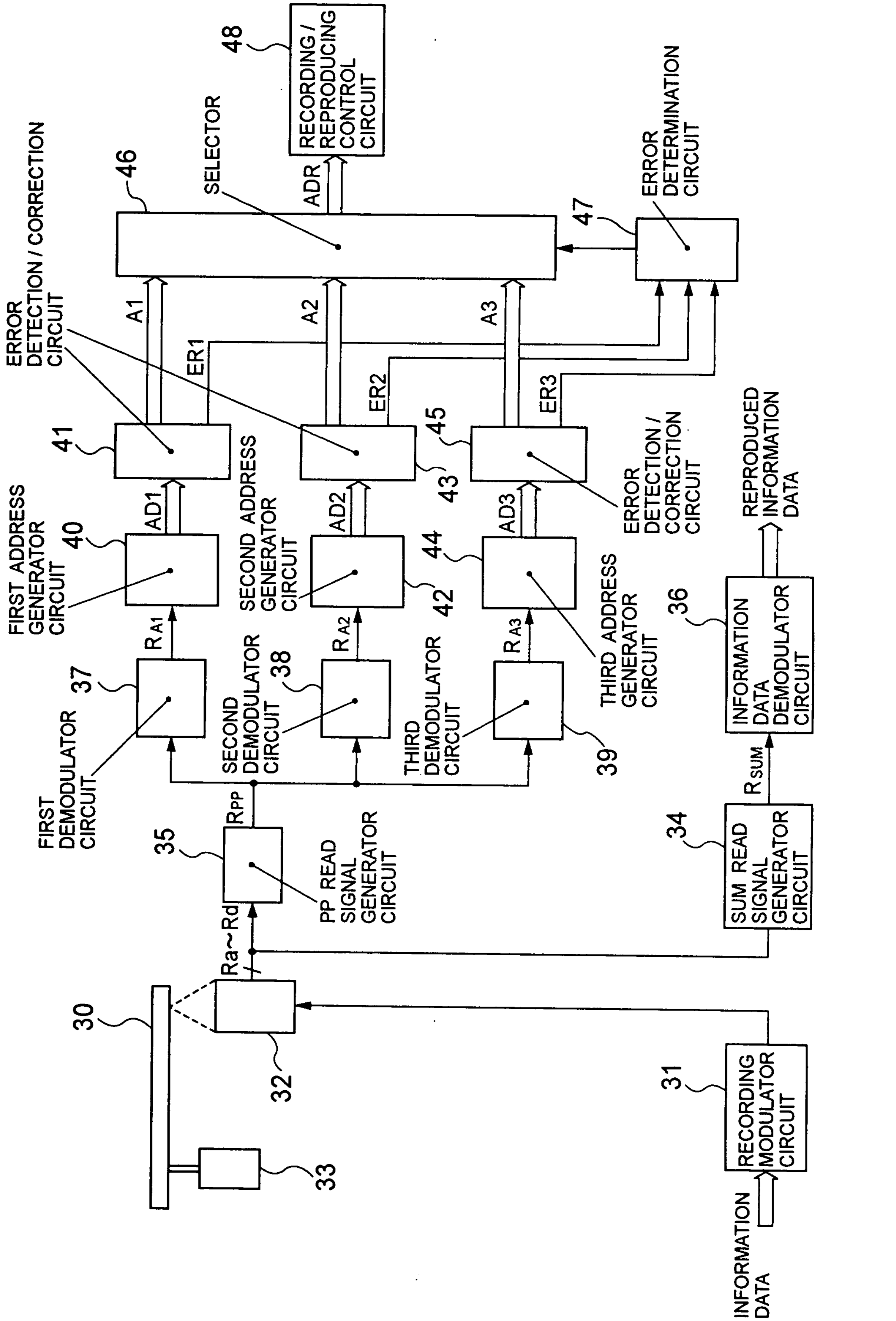

30
33
32
Ra~Rd
35
PP READ SIGNAL GENERATOR CIRCUIT
RPP
FIRST DEMODULATOR CIRCUIT
SECOND DEMODULATOR CIRCUIT
THIRD DEMODULATOR CIRCUIT
37
38
39
RA1
RA2
RA3
FIRST ADDRESS GENERATOR CIRCUIT
SECOND ADDRESS GENERATOR CIRCUIT
THIRD ADDRESS GENERATOR CIRCUIT
40
42
44
AD1
AD2
AD3
41
43
45
ERROR DETECTION / CORRECTION CIRCUIT
ERROR DETECTION / CORRECTION CIRCUIT
A1
A2
A3
ER1
ER2
ER3
46
SELECTOR
ADR
48
RECORDING / REPRODUCING CONTROL CIRCUIT
47
ERROR DETERMINATION CIRCUIT
31
RECORDING MODULATOR CIRCUIT
INFORMATION DATA
34
SUM READ SIGNAL GENERATOR CIRCUIT
RSUM
36
INFORMATION DATA DEMODULATOR CIRCUIT
REPRODUCED INFORMATION DATA

FIG. 4

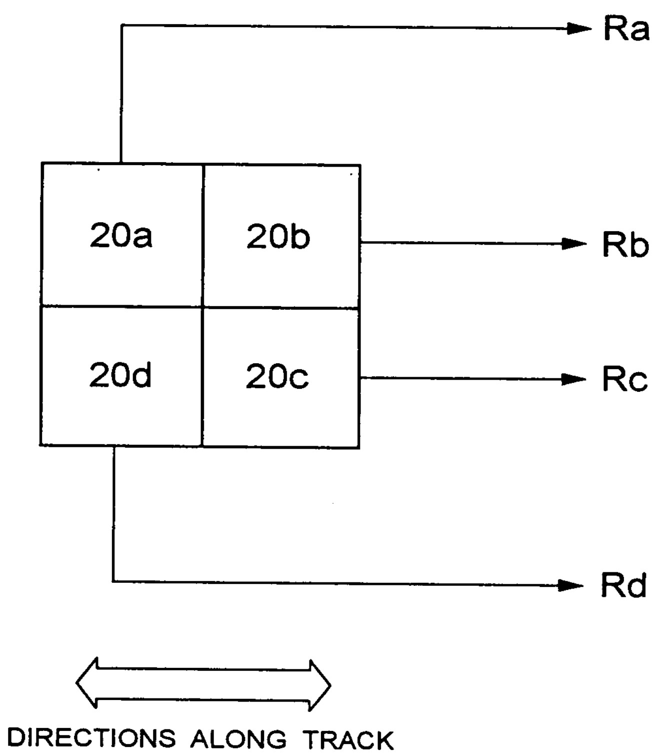


FIG. 5

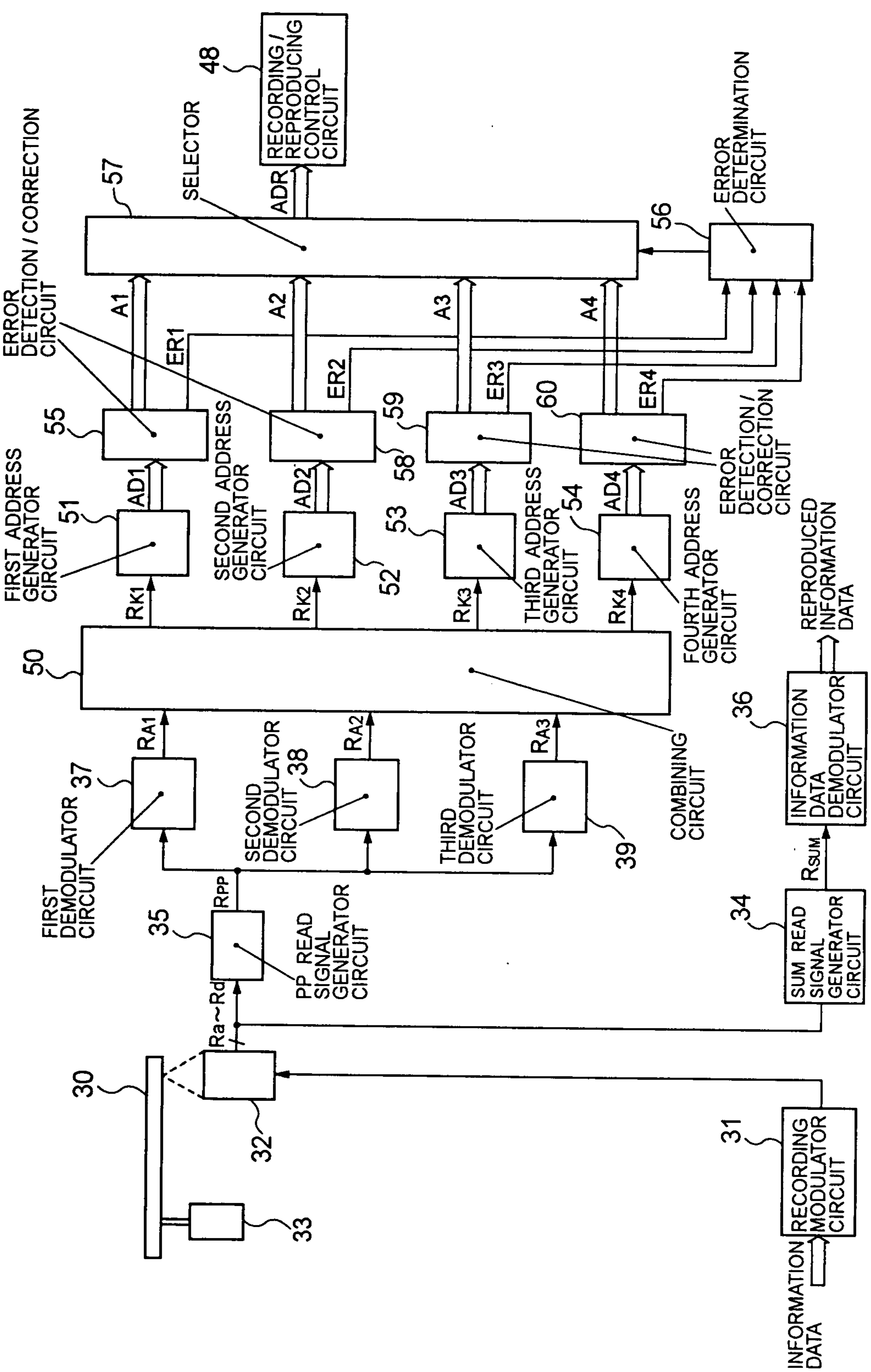

30
32
33
Ra~Rd
35
PP READ SIGNAL GENERATOR CIRCUIT
RPP
FIRST DEMODULATOR CIRCUIT
37
SECOND DEMODULATOR CIRCUIT
38
THIRD DEMODULATOR CIRCUIT
39
RA1
RA2
RA3
50
COMBINING CIRCUIT
RK1
RK2
RK3
RK4
FIRST ADDRESS GENERATOR CIRCUIT
51
SECOND ADDRESS GENERATOR CIRCUIT
52
53
THIRD ADDRESS GENERATOR CIRCUIT
54
FOURTH ADDRESS GENERATOR CIRCUIT
AD1
AD2
AD3
AD4
55
58
59
60
ERROR DETECTION CIRCUIT
ERROR DETECTION/CORRECTION CIRCUIT
A1
A2
A3
A4
ER1
ER2
ER3
ER4
ERROR DETECTION / CORRECTION CIRCUIT
57
SELECTOR
ADR
48
RECORDING / REPRODUCING CONTROL CIRCUIT
56
ERROR DETERMINATION CIRCUIT
34
SUM READ SIGNAL GENERATOR CIRCUIT
RSUM
36
INFORMATION DATA DEMODULATOR CIRCUIT
REPRODUCED INFORMATION DATA
31
RECORDING MODULATOR CIRCUIT
INFORMATION DATA

FIG. 6

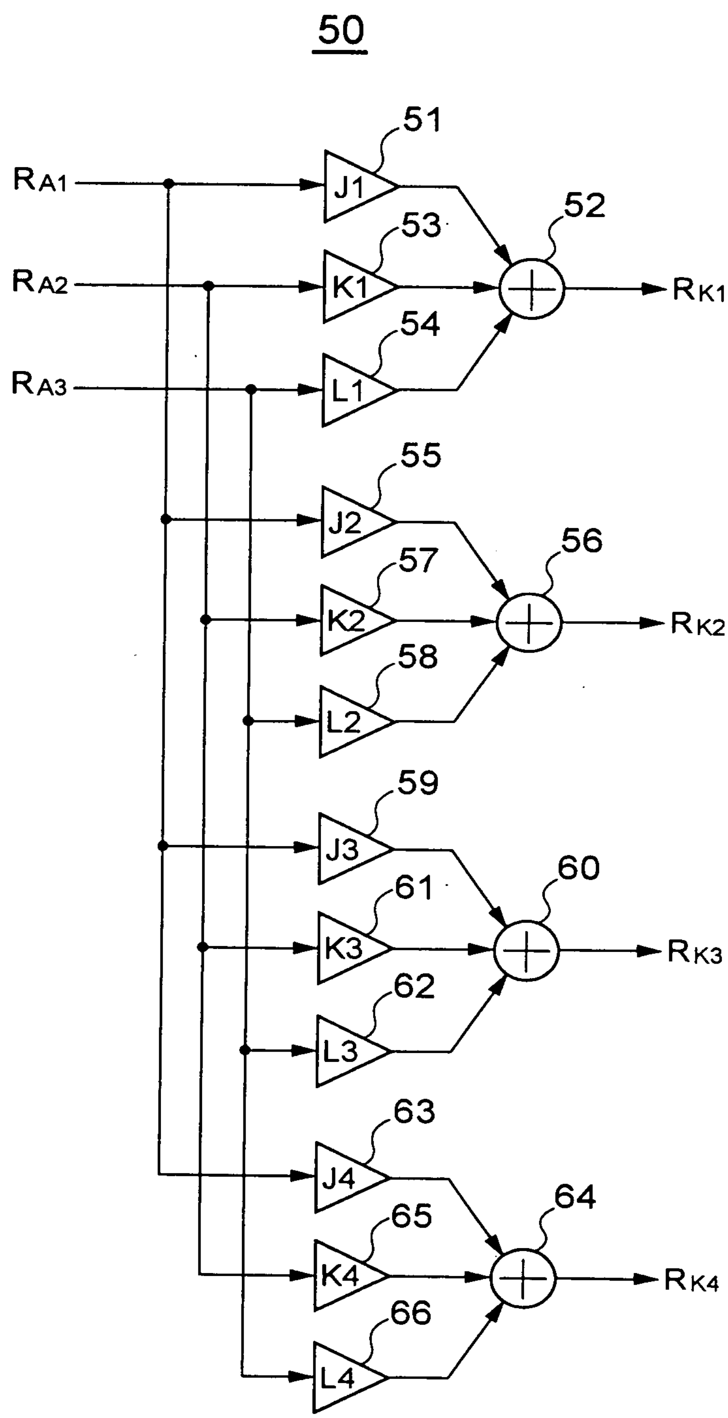
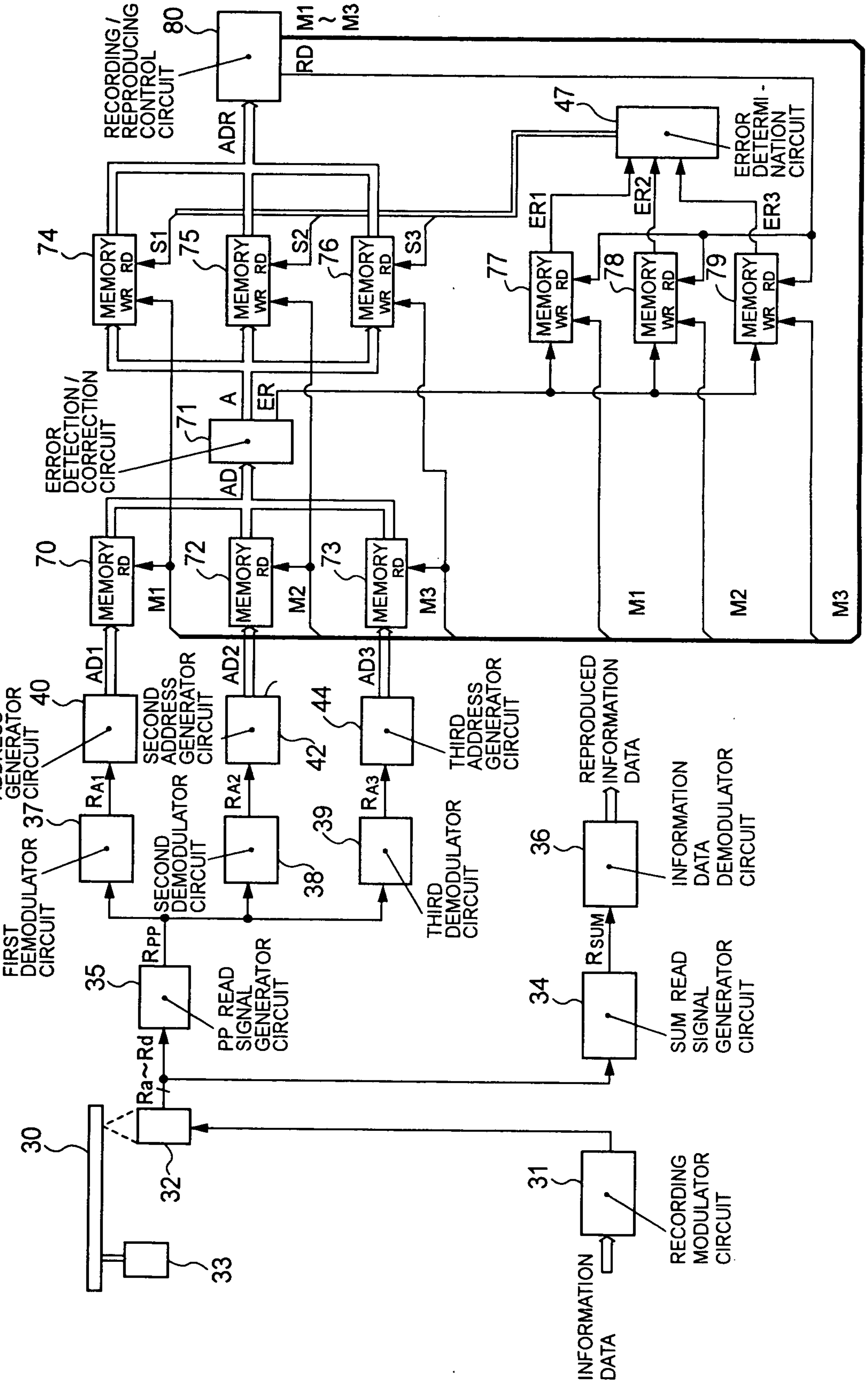

50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
RA1
RA2
RA3
J1
K1
L1
J2
K2
L2
J3
K3
L3
J4
K4
L4
RK1
RK2
RK3
RK4

FIG. 7


30
32
33
Ra~Rd
31
INFORMATION DATA
RECORDING MODULATOR CIRCUIT
35
PP READ SIGNAL GENERATOR CIRCUIT
RPP
34
SUM READ SIGNAL GENERATOR CIRCUIT
RSUM
36
INFORMATION DATA DEMODULATOR CIRCUIT
REPRODUCED INFORMATION DATA
37
FIRST DEMODULATOR CIRCUIT
38
SECOND DEMODULATOR CIRCUIT
39
THIRD DEMODULATOR CIRCUIT
RA1
RA2
RA3
40
FIRST ADDRESS GENERATOR CIRCUIT
42
SECOND ADDRESS GENERATOR CIRCUIT
44
THIRD ADDRESS GENERATOR CIRCUIT
AD1
AD2
AD3
70
72
73
MEMORY RD
M1
M2
M3
AD
71
ERROR DETECTION/ CORRECTION CIRCUIT
A
ER
74
75
76
MEMORY WR RD
S1
S2
S3
77
78
79
ER1
ER2
ER3
47
ERROR DETERMI-NATION CIRCUIT
ADR
80
RECORDING/ REPRODUCING CONTROL CIRCUIT
RD
M1 ~ M3

Appl. No. 10/618,711
Docket No. Q76339
Amdt. Dated October 28, 2003
Replacement Drawings

FIG. 8